CLAIMS

What is claimed is:

1. A method of erasing a core memory cell using a negative gate voltage in a semiconductor memory device, comprising:

generating an erase signal to begin an erase operation;

generating a pre-charge signal according to the erase signal;

pre-charging negative pump MOS regulation capacitors according to the pre-charge signal;

regulating a negative pump voltage using the pre-charged negative pump MOS regulation capacitors; and

erasing the core memory cell by applying a negative gate voltage to the core memory cell using the regulated negative pump voltage.

2. The method of claim 1, wherein generating a pre-charge signal comprises generating a pulse, and wherein pre-charging negative pump MOS regulation capacitors comprises connecting a reference voltage to the negative pump MOS regulation capacitors according to the pulse.

3. The method of claim 2, wherein generating a pre-charge signal comprises generating a pulse having a pulse duration, and wherein pre-charging negative pump MOS regulation capacitors comprises connecting the reference voltage to the negative pump MOS regulation capacitors during the pulse duration.

4. The method of claim 3, wherein the negative pump MOS regulation capacitors comprise a capacitive voltage divider circuit having a first capacitance with a first terminal connected to a ground and a second terminal connected to a switch, and a second capacitance with a first terminal connected to the switch and a second terminal connected to a negative voltage pump, and wherein connecting the reference voltage to the negative pump MOS regulation capacitors during the pulse duration comprises

connecting the reference voltage to the second terminal of the first capacitance and the first terminal of the second capacitance using the switch.

5. The method of claim 4, wherein connecting the reference voltage to the second terminal of the first capacitance and the first terminal of the second capacitance comprises closing the switch according to the pulse.

6. The method of claim 5, wherein the pulse duration is about 160ns.

7. The method of claim 3, wherein the pulse duration is about 160ns.

8. The method of claim 1, wherein pre-charging the negative pump MOS regulation capacitors comprises connecting a reference voltage to the capacitors according to the pre-charge signal.

9. The method of claim 8, wherein pre-charging the negative pump MOS regulation capacitors comprises connecting the reference voltage to the capacitors for about 160ns.

10. The method of claim 1, wherein the negative pump MOS regulation capacitors comprise a capacitive voltage divider circuit having a first capacitance with a first terminal connected to a ground and a second terminal connected to a switch, and a second capacitance with a first terminal connected to the switch and a second terminal connected to a negative voltage pump, and wherein pre-charging the negative pump MOS regulation capacitors connecting a reference voltage to the second terminal of the first capacitance and the first terminal of the second capacitance using the switch.

11. A method of providing a negative gate voltage during a core memory cell erase operation, comprising:

generating a pre-charge signal;

pre-charging negative pump MOS regulation capacitors according to the pre-charge signal;

regulating a negative pump voltage using the pre-charged negative pump MOS regulation capacitors; and

providing a negative gate voltage to the core memory cell using the regulated negative pump voltage.

12. The method of claim 11, wherein generating a pre-charge signal comprises generating a pulse, and wherein pre-charging negative pump MOS regulation capacitors comprises connecting a reference voltage to the negative pump MOS regulation capacitors according to the pulse.

13. The method of claim 12, wherein generating a pre-charge signal comprises generating a pulse having a pulse duration, and wherein pre-charging negative pump MOS regulation capacitors comprises connecting the reference voltage to the negative pump MOS regulation capacitors during the pulse duration.

14. The method of claim 13, wherein the negative pump MOS regulation capacitors comprise a capacitive voltage divider circuit having a first capacitance with a first terminal connected to a ground and a second terminal connected to a switch, and a second capacitance with a first terminal connected to the switch and a second terminal connected to a negative voltage pump, and wherein connecting the reference voltage to the negative pump MOS regulation capacitors during the pulse duration comprises connecting the reference voltage to the second terminal of the first capacitance and the first terminal of the second capacitance using the switch.

15. The method of claim 13, wherein the pulse duration is about 160ns.

16. The method of claim 11, wherein pre-charging the negative pump MOS regulation capacitors comprises connecting a reference voltage to the capacitors according to the pre-charge signal.

17. The method of claim 16, wherein pre-charging the negative pump MOS regulation capacitors comprises connecting the reference voltage to the capacitors for about 160ns.

18. The method of claim 11, wherein the negative pump MOS regulation capacitors comprise a capacitive voltage divider circuit having a first capacitance with a first terminal connected to a ground and a second terminal connected to a switch, and a second capacitance with a first terminal connected to the switch and a second terminal connected to a negative voltage pump, and wherein pre-charging the negative pump MOS regulation capacitors connecting a reference voltage to the second terminal of the first capacitance and the first terminal of the second capacitance using the switch.

19. An apparatus for pre-charging negative pump MOS regulation capacitors during a core cell erase operation in a memory device, comprising:

a switch connected between a reference voltage and the negative pump MOS regulation capacitors; and

a pre-charge control circuit providing a pre-charge signal to the switch;

wherein the switch is operative to selectively connect the reference voltage to the negative pump MOS regulation capacitors according to the pre-charge signal.

20. The apparatus of claim 19, wherein the pre-charge control circuit receives an erase signal during the core cell erase operation, and generates the pre-charge signal for a time period, and wherein the switch connects the reference voltage to the negative pump MOS regulation capacitors during the time period.

21. The apparatus of claim 20, wherein the time period is about 160ns.

22. The apparatus of claim 19, wherein the negative pump MOS regulation capacitors comprise a capacitive voltage divider circuit having a first capacitance with a first terminal connected to a ground and a second terminal connected to the switch, and a second capacitance with a first terminal connected to the switch and a second terminal connected to a negative voltage pump, and wherein the switch is operative to selectively pre-charge the negative pump MOS regulation capacitors by connecting the reference voltage to the second terminal of the first capacitance and the first terminal of the second capacitance according to the pre-charge signal.